Juyeop Baek

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EDUCATION (Applying to PhD Programs in the upcoming cycle)

GEORGIA INSTITUTE OF TECHNOLOGY Atlanta, Georgia
Master of Science in Electrical and Computer Engineering August 2024 – May 2026
GPA: 4.0/4.0

GEORGIA INSTITUTE OF TECHNOLOGY Atlanta, Georgia
Bachelor of Science in Electrical Engineering August 2018 – May 2022
GPA: 3.86/4.0

PROFESSIONAL RESEARCH EXPERIENCE

GRADUATE RESEARCH ASSISTANT, PSYLAB June 2025 – May 2026
GEORGIA INSTITUTE OF TECHNOLOGY Atlanta, Georgia

- Advisor: Dr. Visvesh Sathe
- Thesis Title: Methodologies for Automated Power Delivery Network Extraction in Heterogeneous 2.5D/3D Packaging
- Automated PDN extraction flows for advanced packaging systems, optimizing granularity and power integrity analysis from VR and decoupling capacitor placement
- Constructed and examined end-to-end VR-to-load PDN models, comparing side-mounted, backside, and land-side architectures for efficiency

GRADUATE RESEARCH ASSISTANT, GTCAD August 2024 – May 2025
GEORGIA INSTITUTE OF TECHNOLOGY {Relocated to University of Southern California}

- Advisor: Dr. Sung Kyu Lim
- Created and verified EDA flows for advanced packaging systems in chiplet partitioning, placement, routing, and integrity/reliability testing
- Utilized deep reinforcement learning for S/P/T integrity and delay simulations' speedup, prediction, and optimization

UNDERGRADUATE RESEARCH ASSISTANT, GAMMA LABORATORY August 2020 – May 2022
GEORGIA INSTITUTE OF TECHNOLOGY Atlanta, Georgia

- Advisor: Dr. Shaolan Li
- Created an RTL-to-GDSII tool flow for a delta-sigma analog-digital converter made completely from EDA - friendly digital cells
- Leveraged Synopsys and Cadence software to generate and modify floorplans from Verilog descriptions while optimizing timing, area, and power

PUBLICATIONS

[1] Seungmin Woo, **Juyeop Baek**, Pruek Vanna-iampikul, Srujan Penta, Per Viklund, Yang Fan, Bongyoung Yoo and Sung Kyu Lim, "AI-Driven Wire Sizing for Signal Integrity Optimization in 2.5D ICs with Nickel-Iron Interconnects ", in Proc. Design, Automation and Test in Europe Conf. (DATE), 2026

[2] Jin Woong Kwak*, **Juyeop Baek***, Muhannad Bakir, Visvesh Sathe, “Modeling and Optimization of 2-stage Power Delivery Systems for High-Performance, Large-Area Packages”, *IEEE 76th Electronic Components and Technology Conference (ECTC)*, 2026 (*Equal Contribution)

TEACHING EXPERIENCE

Georgia Institute of Technology – Teaching Assistant (2020 – 2022)

- *Digital Design Laboratory:* Design and implementation of digital systems, including a FPGA-based hardware design project. CAD tools, project design methodologies, logic synthesis, and assembly language programming
- *Measurements, Circuits, and Microelectronics Laboratory:* Theory and experiments related to the design, analysis, construction, and measurement of elementary passive and active analog circuits using both discrete and integrated devices
- *Intro Physics II:* A calculus-based course with laboratory covering electromagnetism, applications of light and modern physics

PROFESSIONAL EXPERIENCE

PARTNERSHIP FOR AN ADVANCED COMPUTING ENVIRONMENT August 2025 – Present
Georgia Institute of Technology Atlanta, Georgia

- Assisted in the management and development of over 1000 GPU-enabled HPC datacenter for research and class usage
- Created various MIG and sharding scripts for an efficient workload partition and monitoring for efficient power consumption while allowing multiple concurrent processes

HARDWARE ENGINEERING INTERN, SAMSUNG ELECTRONICS June 2024 – August 2024
Mobile eXperience Division, Display Group Suwon, South Korea

- Specialized in the design of the display driver interface chip
- Created pass transistor and dynamic logic variations of circuits for higher propagation speed and lower power consumption

CONSULTANT INTERN, DELOITTE March 2024 – June 2024
Monitor Deloitte, Consulting Division Seoul, South Korea

- Conducted extensive research and analysis on the current state of the AI accelerator market, as well as the emerging new technologies
- Assisted in the development of client proposals and presentations by streamlining data collection processes

SKILLS

Programming	C++, CUDA, Python, Bash, Tcl, SKILL, Verilog, VHDL, MATLAB
CAD	Cadence: Genus, Innovus, Virtuoso, APD
	Synopsys: Design Compiler, IC Compiler II, PrimeSim, HSPICE
	Siemens: Xpedition Enterprise, Hyperlynx, Calibre, Mentor Graphics
	Ansys: Electronics Desktop Suite, SiWave, Lumerical
	Keysight ADS
Hardware	FPGAs, Spectrum Analyzers, Oscilloscopes, Microcontrollers
Languages	English(Native), Korean(Native)

AWARDS & FUNDING

- SRC Scholar (JUMP 2.0 CHIMES) 2024 - Present
- Faculty Honors 2018 - 2022
- Dean's List 2018 - 2022

PROFESSIONAL MEMBERSHIPS

- Georgia Tech IEEE Chapter 2018 – 2022

LEADERSHIP AND SERVICE

- Chair, Georgia Tech IEEE Chapter August 2019 – May 2022
- Signal Intelligence Leader, Republic of Korea Army September 2022 – March 2024